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CMPE 415

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Homework 4 Report

Statement of Project Completion

My project works to about full completion. Each functionality of the CPU depending on the op code work to the fullest degree. I was able to complete all the files that were asked for in the project. The completed files include:

* ALU Block Diagram(Phase 1)
* ALU packaged IP(Phase 1)
* ISA\_decode
* Register\_File
* MUX
* SSD(with sub-files listed later in the report)
* Debounce\_cb
* tb\_ISA\_decode

Description of each module

* **ISA\_decode:** This module is basically the top of the whole CPU. It decodes the input from the FPGA switches. The SSD, register\_file and debounce\_cb modules.   
  The main goal for this module is to take the op code from the switches input and decide what it needs to do
* **register\_file:** This module is where 16 16-bit registers are held. It also sets the value of rs\_data and rd\_data using the output of the MUX module. This is where are the values of the registers stored.
* **MUX:** This module maps the outputs from the ALU to respectively named wires and takes in the opcode from the ISA. Using the opcode it decides which value from the ALU it needs to send to the register\_file module.
* **SSD:** No files were provided for the SSD thus I had to use online resources. I was able to create my SSD hierarchy from watching this video here -> https://www.youtube.com/watch?v=v2CM8RaEeQU
  + I was able to map the Anode and Cathode outputs to RD and RS from the SSD module.
* **clk\_divider(SSD sub-module):** This module takes in the system given Clk frequency and makes the clock slower in order for the refresh counter to use.
* **refresh\_clk(SSD sub-module):** This module outputs a refresh\_out value that changed on the refresh\_clk value. This value is used to decide which anode will be turned on.
* **anode\_control(SSD sub-module):** This module will turn on the specific anode depending on the refresh\_clk value.
* **BCD\_on (SSD sub-module):** This module outputs a value depending on the refresh\_clk which is in sync with the anode module. This means the output value is for the anode that is currently on.
* **cathode(SSD-module):** This module takes in the value from the BCD\_on module and displays it by changing the value into cathode values.
* **Debounce\_cb:** This module is just a debounce for the center button.
* **tb\_ISA\_decode:** This is the test bench for the whole CPU. It gives specific values for the switch inputs for the ISA\_decode module to test the CPU.

Block Diagram for CPU

This is the block diagram of my implementation of the CPU. The clk input while only shown as an input to clk\_divider, is also an input to all the other modules not associated with the SSD.

